

B2B Connector for CPU Board

DF40C(2.0)-80DS-0.4V(S)/0.4mm-Hirose

CN1

DF40C-100DP-0.4V(51)

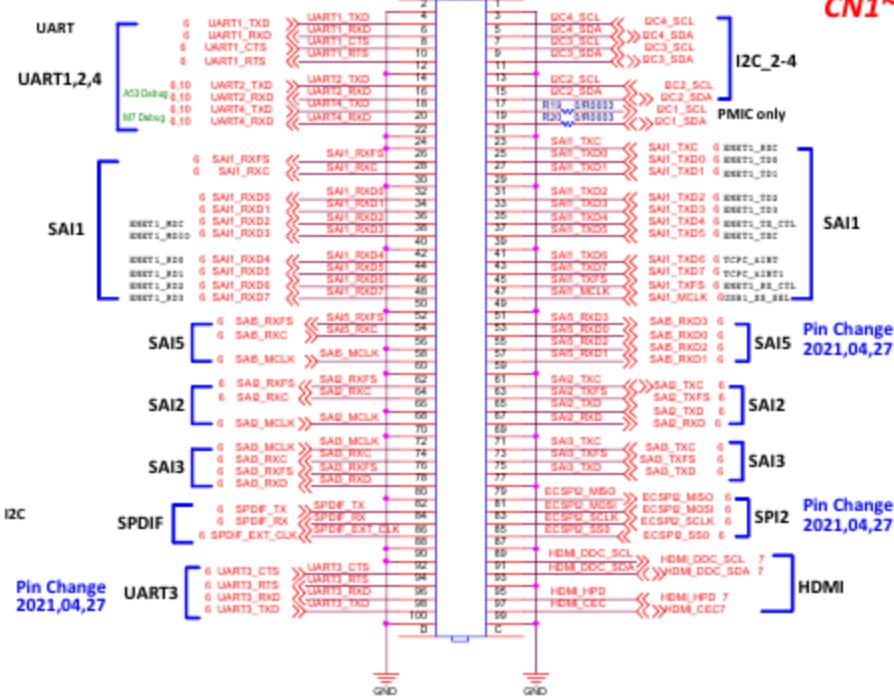
Header

DF40C-60DP-0.4V/0.4mm-Header

CN1~CN4 = Odd PIN is inside in Bottom SIDE

Header

CN3



J5 -----> CN1
J6 -----> CN2
J3 -----> CN3
J4 -----> CN4

Header

Ethernet
Pin Change
2021.04.27

SDIO2
Pin Change
2021.04.27

Pin-to-pin comparison diagram for the ENEC1000 and ENEC1000C1000. The diagram shows two columns of pins, one for the ENEC1000 (left) and one for the ENEC1000C1000 (right). Pins are numbered 1 to 100. Pins 1-33 are ENEC1000-specific, pins 34-46 are shared, and pins 47-100 are ENEC1000C1000-specific. Power pins VDD_3V3, VSD_3V3, and VSYS_5V are shown on both sides. The diagram is a direct pin-to-pin comparison, showing that the pin functions are identical for the shared pins.

Pin	ENE1000	ENE1000C1000
1	ENET_MD0	ENET_MD0
2	ENET_MD1	ENET_MD1
3	ENET_MD2	ENET_MD2
4	ENET_MD3	ENET_MD3
5	ENET_MD4	ENET_MD4
6	ENET_MD5	ENET_MD5
7	ENET_MD6	ENET_MD6
8	ENET_MD7	ENET_MD7
9	ENET_MD8	ENET_MD8
10	ENET_MD9	ENET_MD9
11	ENET_MD10	ENET_MD10
12	ENET_MD11	ENET_MD11
13	ENET_MD12	ENET_MD12
14	ENET_MD13	ENET_MD13
15	ENET_MD14	ENET_MD14
16	ENET_MD15	ENET_MD15
17	ENET_MD16	ENET_MD16
18	ENET_MD17	ENET_MD17
19	ENET_MD18	ENET_MD18
20	ENET_MD19	ENET_MD19
21	ENET_MD20	ENET_MD20
22	ENET_MD21	ENET_MD21
23	ENET_MD22	ENET_MD22
24	ENET_MD23	ENET_MD23
25	ENET_MD24	ENET_MD24
26	ENET_MD25	ENET_MD25
27	ENET_MD26	ENET_MD26
28	ENET_MD27	ENET_MD27
29	ENET_MD28	ENET_MD28
30	ENET_MD29	ENET_MD29
31	ENET_MD30	ENET_MD30
32	ENET_MD31	ENET_MD31
33	ENET_MD32	ENET_MD32
34	SD2_WP	SD2_WP
35	SD2_CD	SD2_CD
36	SD2_CMD	SD2_CMD
37	SD2_CLK	SD2_CLK
38	SD2_WP	SD2_WP
39	SD2_CD	SD2_CD
40	SD2_CMD	SD2_CMD
41	SD2_CLK	SD2_CLK
42	SD2_WP	SD2_WP
43	SD2_CD	SD2_CD
44	SD2_CMD	SD2_CMD
45	SD2_CLK	SD2_CLK
46	SD2_WP	SD2_WP
47	SD2_CD	SD2_CD
48	SD2_CMD	SD2_CMD
49	SD2_CLK	SD2_CLK
50	SD2_WP	SD2_WP
51	SD2_CD	SD2_CD
52	SD2_CMD	SD2_CMD
53	SD2_CLK	SD2_CLK
54	SD2_WP	SD2_WP
55	SD2_CD	SD2_CD
56	SD2_CMD	SD2_CMD
57	SD2_CLK	SD2_CLK
58	SD2_WP	SD2_WP
59	SD2_CD	SD2_CD
60	SD2_CMD	SD2_CMD
61	SD2_CLK	SD2_CLK
62	SD2_WP	SD2_WP
63	SD2_CD	SD2_CD
64	SD2_CMD	SD2_CMD
65	SD2_CLK	SD2_CLK
66	SD2_WP	SD2_WP
67	SD2_CD	SD2_CD
68	SD2_CMD	SD2_CMD
69	SD2_CLK	SD2_CLK
70	SD2_WP	SD2_WP
71	SD2_CD	SD2_CD
72	SD2_CMD	SD2_CMD
73	SD2_CLK	SD2_CLK
74	SD2_WP	SD2_WP
75	SD2_CD	SD2_CD
76	SD2_CMD	SD2_CMD
77	SD2_CLK	SD2_CLK
78	SD2_WP	SD2_WP
79	SD2_CD	SD2_CD
80	SD2_CMD	SD2_CMD
81	SD2_CLK	SD2_CLK
82	SD2_WP	SD2_WP
83	SD2_CD	SD2_CD
84	SD2_CMD	SD2_CMD
85	SD2_CLK	SD2_CLK
86	SD2_WP	SD2_WP
87	SD2_CD	SD2_CD
88	SD2_CMD	SD2_CMD
89	SD2_CLK	SD2_CLK
90	SD2_WP	SD2_WP
91	SD2_CD	SD2_CD
92	SD2_CMD	SD2_CMD
93	SD2_CLK	SD2_CLK
94	SD2_WP	SD2_WP
95	SD2_CD	SD2_CD
96	SD2_CMD	SD2_CMD
97	SD2_CLK	SD2_CLK
98	SD2_WP	SD2_WP
99	SD2_CD	SD2_CD
100	SD2_CMD	SD2_CMD

[illegible]

MIPI-CSI_CH2

PMIC

CLK

QSPI 64

CN4

Header

