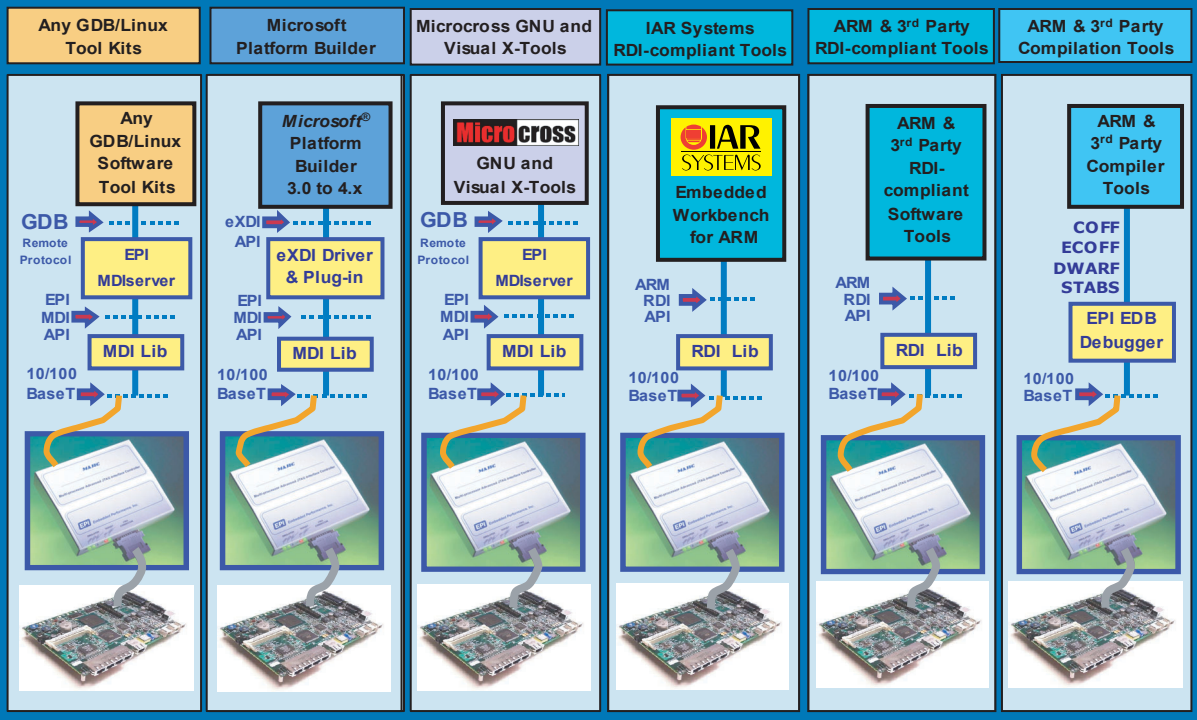
# 임베디드 시스템 개발툴 솔루션


공급업체 : Embedded System Leader

Micro Vision (주)마이크로비전

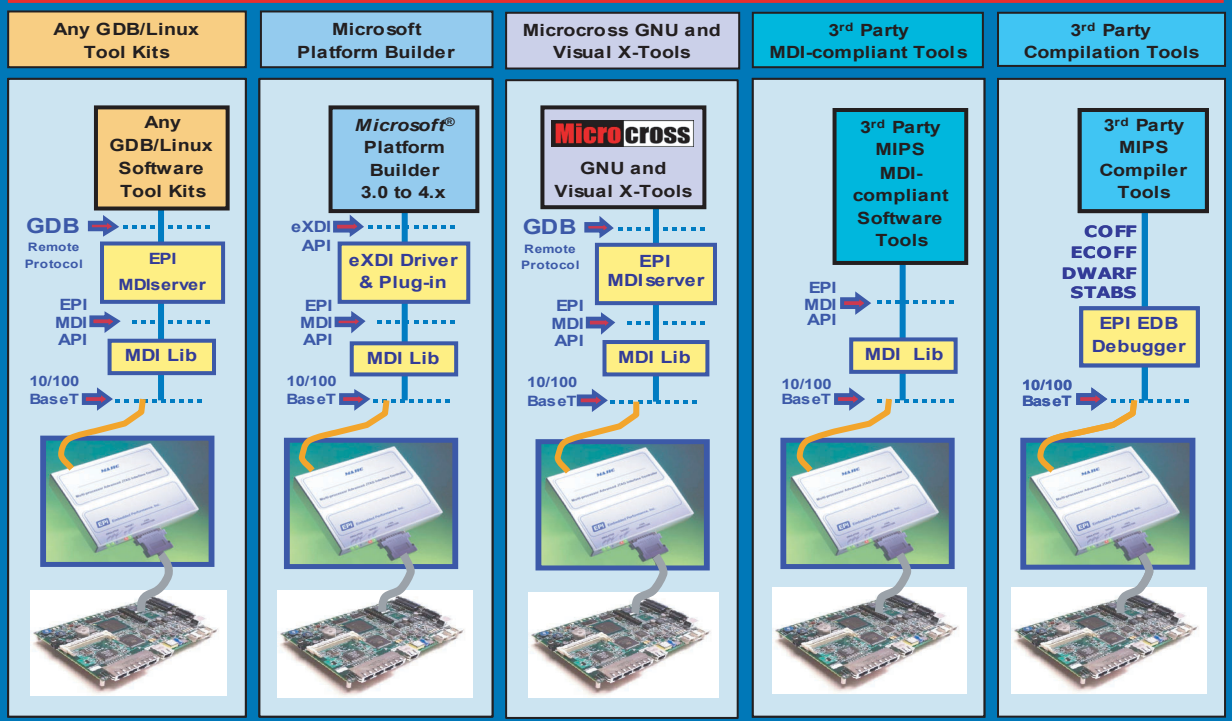
# ARM 개발장비 JTAG 에뮬레이터 & 디버거

## EPI Development Environments for ARM



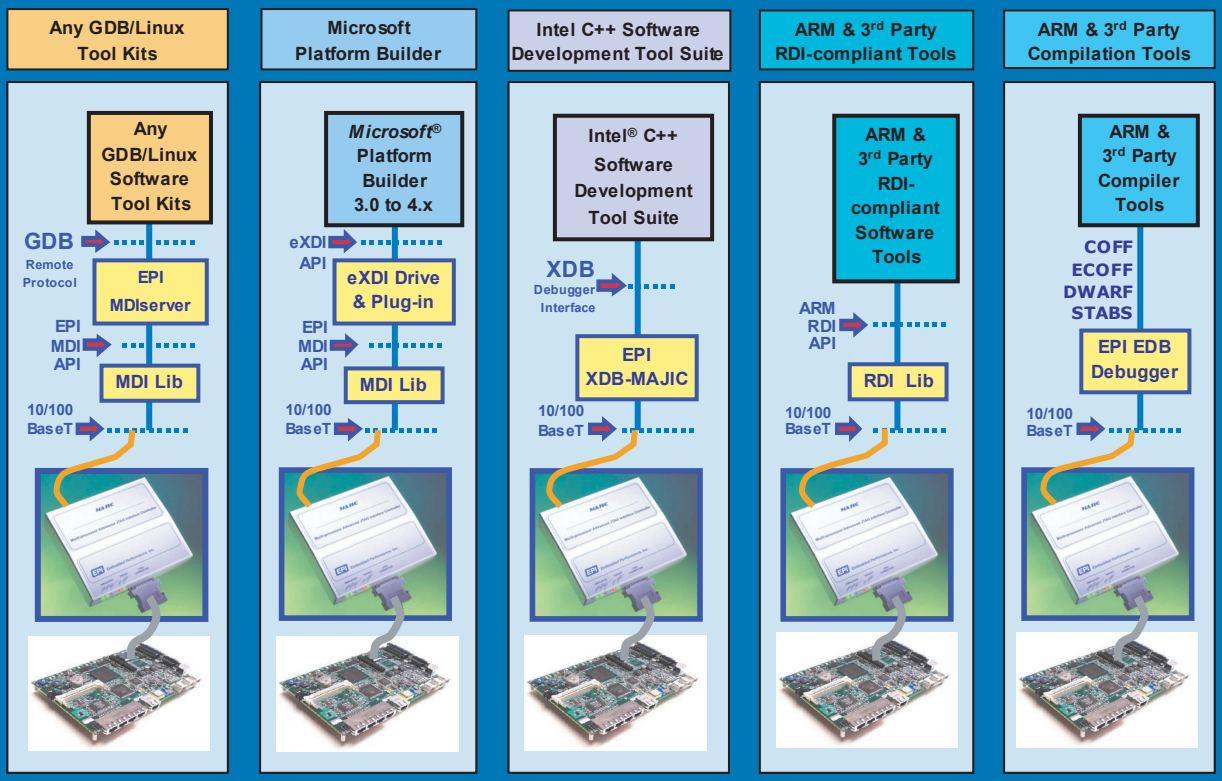

# MIPS 개발장비 JTAG 에뮬레이터 & 디버거

## EPI Development Environments for MIPS



# XScale JTAG 에뮬레이터 & Intel SDT 컴파일러

## EPI Development Environments for XScale

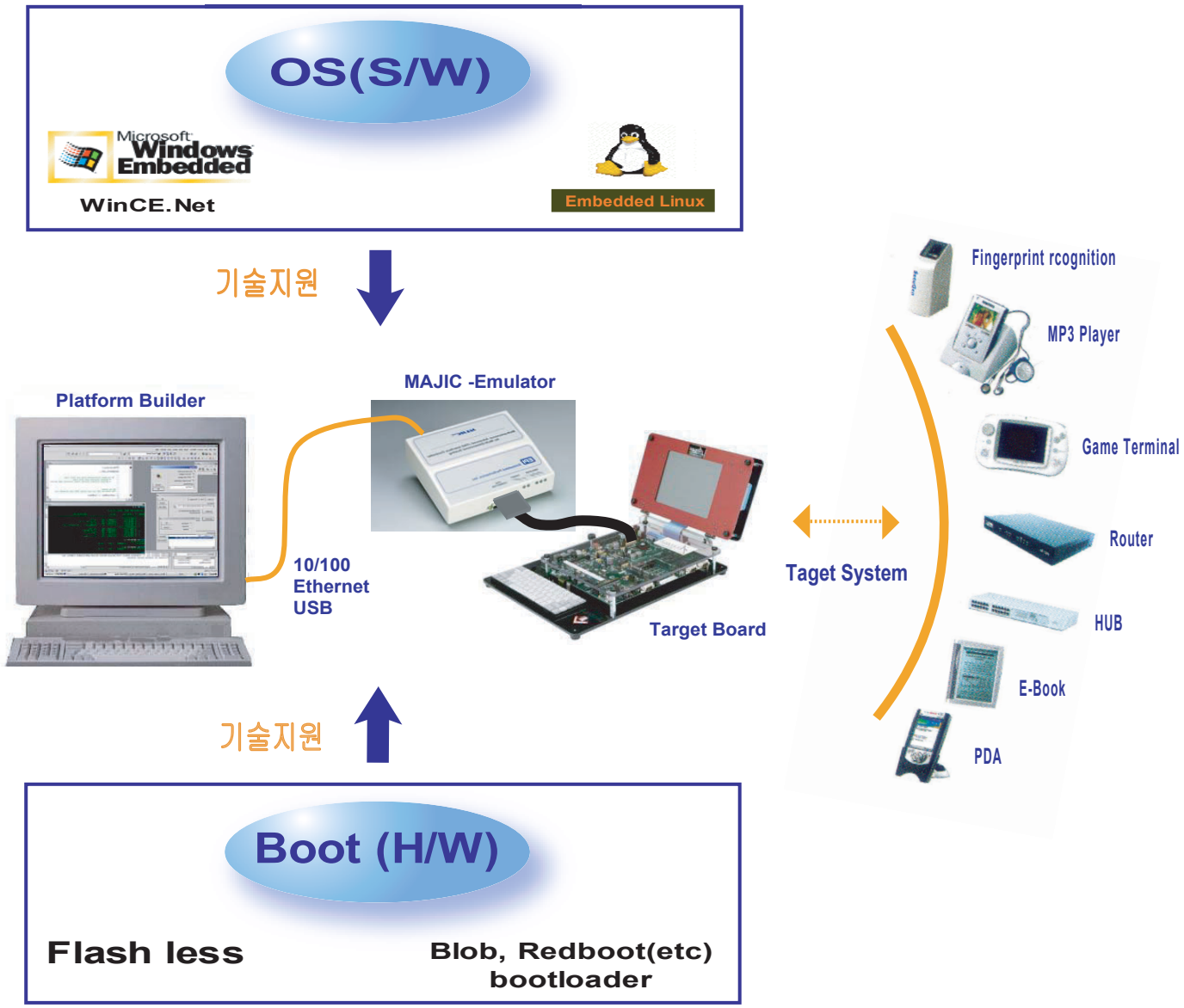


# ARM / Xscale / Mips 개발장비 JTAG 에뮬레이터

## (Mips/Xscale/ARM지원 )

### 최상의 RISC 시스템 개발 솔루션

-개발 Target 최적의 Emulator
-Powerful한 EDB 운용 S/W Package
-기능 : On-Chip Traice, 리눅스/ WinCE.Net O/S 완벽지원, 멀티코아/ 타스킹/ 프로세서
-기술지원 : H/W셋팅, 플래시 다운로딩 및 Bootload 까지 지원
-칩지원 : Xscale / ARM / Mips 그외 다수
-Flash 지원 리스트 : Intel, AMD, Toshiba, Atmel, Micronix, SST, Fujitsu
ST Microelectronics, Mitsubishi, Sharp, MCP, etc...




제조업체 : Risc칩 20년 전통의 자존심 (U.S.A)
EPI Embedded Performance, Inc.

공급업체 : Embedded System Leader
Micro Vision (주)마이크로비젼

# MAJIC III™ Multi-processor Advanced JTAG Interface Controller

## MAJIC III™ JTAG Emulator :

- **Non-intrusive, uses no target resources**
- **Supports specific on-chip debug interfaces**
- **Supports specific CPU core(s)**
- **Supports on-chip hardware breakpoints**
- **Unlimited software breakpoints**
- **Programmable JTAG clock**
- **Ethernet, USB and serial I/O ports for fast, flexible host interface**
- **High speed download of application code**
- **Network compatibility allows shared and remote operation**
- **Internal RISC processor provides intelligent target control**
- **Internal Flash memory for easy firmware update**
- **Sleep-mode support** (Except for Intel® XScale™ CPU cores)
- **LEDs display operation status**
- **ARM/Xscale/Mips**
- **Manufacture : EPI Inc (USA)**


**< MODEL : MAJIC III >**

- **MDI Meta Debugger Interface (for MIPS, ARM and XScale tools)**
- **RDI Remote Debugger Interface (ARM)**
- **eXDI for Platform Builder**
- **MDIserver translates GDB remote to MDI debug service requests to MAJIC III™**

## Major features of the MAJIC III ™ include:

### Ethernet Interface

The 10Base-T/100Base-T Ethernet interface provides many advantages over serial or parallel interfaces to the host. Download of your application code is over ten times faster than with serial interface. This will significantly reduce the amount of time spent waiting for code changes to download to your target board.

Network connection allows remote operation of the MAJICIII™. Now you can access the lab setup directly from your desktop. This allows multiple engineers to share a common test bench.

### Flash Memory

The MAJICIII™ firmware is easily upgraded without the need to replace ROMs.

Install new configuration kits easily and quickly to add support for multiple CPU types with a simple firmware upgrade.

Use the simple program provided to automatically program the updated firmware into the on-board flash memory.

Flash memory also makes it easy to program an IP address into the MAJICIII™ for point-to-point Ethernet connection to a PC or workstation.

### Internal RISC Processor

The use of a high performance internal RISC processor allows fast response to debugger operations such as single-stepping and downloading of application code to the target.

### Status LEDs

The MAJICIII™ provides two LEDs, which show the operational status of the emulator.

### Choice of Configuration Kits

You may configure the MAJICIII™ to support one or more of the supported combinations of CPU core and on-chip debug interface. Each configuration kit includes the firmware, user license and interconnections necessary to support the CPU that you have chosen. Please refer to the Configuration Kit data sheet for detailed specifications on the CPUs and on-chip interfaces currently supported.

### Programmable JTAG Clock

The MAJICIII™ features a programmable TCK with a 0 to 10 MHz range. This allows you to tailor the JTAG operation to match the performance of your target. It also means that you can use the MAJICIII™ with low speed ASIC emulators, with FPGA implementation of your SoC design, or with devices that feature sleep mode operation.

### Convenient Reset Switch

A convenient reset button on the MAJICIII™ is protected against accidental activation, yet is easily accessible by the user when a complete system reset is desired.

### International Power Supply

The MAJICIII™ operates from a standard 5V power source. It comes with an external UL/CE approved AC adapter whose AC input range is compatible with all international AC voltage and frequency ranges. A standard three-wire power connector is compatible with readily available power cords through the world.

### Specifications:

#### MAJIC III™

| | |
|---|---|
| JTAG clock(TCK): | 0 to 10 MHz, programmable |
| Download speed: | >100k bytes/sec (typical) |
| Target voltage: | 3.3V |
| Serial interface: | RS232C 1900-115.2k baud |
| Ethernet interface: | 10/100base-T, TCP/IP |
| USB: | USB 2.0 (Ethernet-to-USB Adapter – Refer to Application Note) |
| Indicator LEDs: | Power, status, Ethernet |
| Size: | 2.0 H x 7.4 W x 6.5 L (inches) |
| Weight: | 1.5 lbs |
| Input power: | 9 VDC +/- 5%, 2.0 A |
| Power connector: | 1.7 mm coaxial, center positive, male |
| Temperature: | Operating 0 - 40 degrees C |
| Humidity: | Operating 15% - 95% RH |

#### External AC Adapter

| | |
|---|---|
| Output: | 9 VDC, 2.0 A |
| Input voltage: | 90 - 264 VAC |
| Input frequency: | 47 - 63 Hz |
| Input power: | 0.6 A |
| Size: | $1.^{1/8}$ H x $1.^{7/8}$ W x 4.25 L (inches) |
| Weight: | 6 oz |
| Compliance: | UL, CUL, CE, TUV |
| AC connector: | EN 60320/13 |
| DC connector: | 1.7 mm coaxial, center positive, female |

# MAJIC™ Multi-processor Advanced JTAG Interface Controller

## MAJIC Development System Features:

- **Ideal for SoC based applications**
- **Non-intrusive, uses no target resources**
- **Supports a wide choice of on-chip debug interfaces**
- **Supports a wide variety of CPU cores**
- **Supports on-chip hardware breakpoints**
- **Unlimited software breakpoints**
- **Programmable JTAG Clock (TCK = 0 to 40 MHz)**
- **Programmable trigger-in and trigger-out connections**
- **Ethernet and Serial I/O Ports for fast, flexible host interface**
- **High speed download (>200k bytes per second) of application code**
- **Network compatibility allows shared and remote operation**
- **Internal RISC Processor assures fast operation**
- **Flash Memory for easy firmware updates to support for additional CPU cores or on-chip debug interfaces.**
- **External AC adapter compatible with all international power sources**
- **Support Risc : Xscale / ARM / MIPS**


MAJIC

- **Sleep-mode support**
- **LED's display operation status**
- **Open API for debugger interface**
- **EDB integrated debugger**

## Major features of the MAJIC include:

### Ethernet Interface

The 10base-T/100base-T Ethernet interface provides many advantages over serial or parallel interfaces to the host. Download of your application code is over ten times faster than with serial interface. This will significantly reduce the amount of time spent waiting for code changes to download to your target board.

Network connection allows remote operation of the MAJIC. Now you can access the lab setup directly from your desktop. This allows multiple engineers to share a common test bench.

### Flash Memory

The MAJIC firmware is easily upgraded without the need to replace ROMs.

Install new configuration kits easily and quickly using the simple program provided. You can add support for multiple CPU types to the MAJIC with a simple firmware upgrade.

New firmware updates will be available on the our FTP site. Use the simple program provided to automatically program the updated firmware into the on-board flash memory.

Flash memory makes it easy to program an IP address into the MAJIC for point-to-point ethernet connection to a PC or workstation.

### Internal RISC Processor

The use of a high performance internal RISC processor allows fast response to debugger operations such as single stepping, reading and writing memory, reading and writing registers, and downloading of application code to the target.

### MAJIC$^{PLUS}$ Version Includes Trace

For a version that includes execution tracing, see the MAJIC$^{PLUS}$ data sheet.

### Status LEDs

The MAJIC provides five LEDs which show the operational status of the emulator. These LEDs also indicate the results of the built-in self test that is automatically performed upon startup.

### Choice of Configuration Kits

You may configure the MAJIC to support one or more of the supported combinations of CPU core and on-chip debug interface. Each configuration kit includes the firmware, user license and interconnections necessary to support the CPU that you have chosen. Please refer to the Configuration Kit data sheet for detailed specifications on the CPUs and on-chip interfaces currently supported.

### Programmable JTAG Clock

The MAJIC features a programmable TCK with a 0 to 40 MHz range. This allows you to tailor the JTAG operation to match the performance of your target. It also means that you can use the MAJIC with low speed ASIC emulators or with devices that feature sleep mode operation.

### Convenient Reset Switch

A convenient reset button on the MAJIC is protected against accidental activation, yet is easily accessible by the user when a complete system reset is desired.

### Programmable Trigger Control

The MAJIC provides the user control over both the trigger-in and trigger-out signals. The trigger-in signal may be used to create a breakpoint or synchronize execution. A trigger output may be set to define execution status, indicate memory accesses, or indicate a memory test failure.

### International Power Supply

The MAJIC operates from a standard 5V power source. It comes with an external UL/CE approved AC adapter whose AC input range is compatible with all international AC voltage and frequency ranges. A standard three-wire power connector is compatible with readily available power cords through the world.

### Specifications:

***MAJIC***

| | |
|---|---|
| JTAG clock(TCK): | 0 to 40 MHz Programmable |
| Trace clock(DCK): | 0 to 100MHz (MAJIC$^{PLUS}$) |
| Download Speed: | >200k bytes/sec (Typical) |
| Target voltage: | 1.8~5.0V |
| Serial interface: | RS232C 1900-115.2k baud |
| Ethernet interface: | 10/100Base-T, TCP/IP |
| Triggers: | Trigger input Trigger output |
| Trigger Control | |
| Trigger In: | Off, Run sync, Break |
| Trigger Out: | Off, Run sync, Memory access, Memory test error |
| Trigger Levels: | TTL |
| Indicator LEDs: | Power, Status, Run, Connect. Ethernet |
| Size: | 2.0 H x 7.4 W x 6.5 L (inches) |
| Weight: | 2.25 lbs |
| Input power: | 5 VDC +/- 5%, 4.0 A |
| Power connector: | 2.1 mm coaxial, center positive, male |
| Temperature: | Operating 0 - 40 degrees C |
| Humidity: | Operating 15% - 95% RH |
| Safety/EMC | CE |

***External AC Adapter***

| | |
|---|---|
| Output: | 5 VDC, 4.0 A |
| Input voltage: | 90 - 264 VAC |
| Input frequency: | 47 - 63 Hz |
| Input power: | 0.8 A |
| Size: | 1.6 H x 2.8 W x 4.8 L (inches) |
| Weight: | 10.3 oz |
| Compliance: | UL, CUL, CE, TUV |
| AC connector: | EN 60320/13 |
| DC connector | 2.1 mm coaxial, center positive, female |

## M A J I C MX for Intel® XScale™ MicroArchitecture :

- Ideal for Intel XScale based applications
- Supports the Intel PXA210/250 applications processors, IOP310/321 I/O processors, and IXP425/2400/2800 and IXP1100 Network processors, Bulverde
- 10/100Base-T Ethernet and serial I/O ports for fast, flexible host interface
- Supports the Intel XScale on-chip trace
- Programmable JTAG clock (TCK = 2kHz to 40MHz)
- Programmable trigger-in and trigger-out connections
- Ethernet and serial I/O ports for fast, flexible host interface
- High-speed download of application code
- Network compatibility allows shared and remote operation
- Works with EDB, or third party RDI 1.5.1 compliant debuggers
- Wind River Tornado BackEnd Support
- Proven to work with Intel DBPXA250, IQ80310, IQ80321, ADI 80200EVB, BRH Development Platform...etc.
- Unlimited software breakpoints

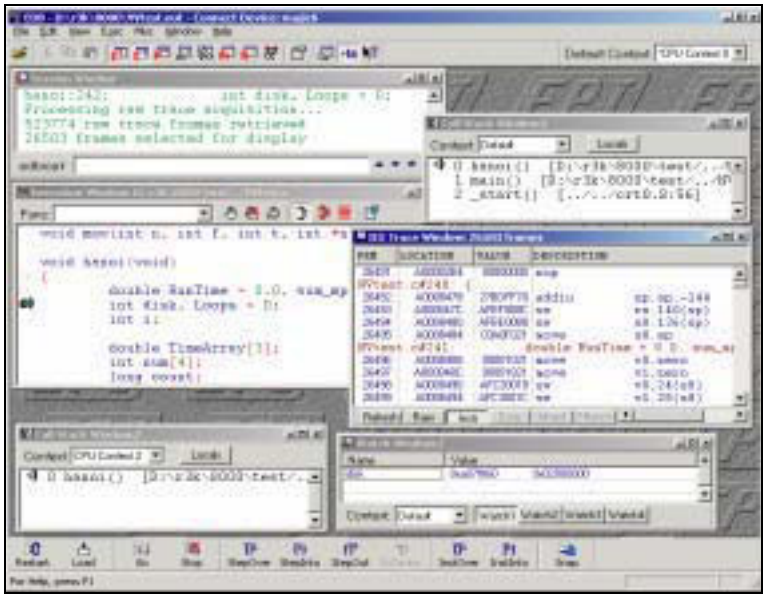
M A J I C MX™

- Non-intrusive, uses no target resources
- LEDs display operational status
- Supports on-chip hardware breakpoints

# EDB Source-level Debugger

## Key Features of EDB:

- Extensive Set of GUI Debugger Window Types
- Compatible with a wide selection of compilers including: EPI, ARM, GNU-gcc, Mentor, Metaware, MontaVista-gcc, Wind River gcc and Diab.
- Sophisticated Breakpoint Control Features
- Supports the Most Extensive List of ARM, MIPS, and Intel XScale Cores in the Industry
- Customizable RTOS Support
- Extensible Debugger Command Language
- Multiple Context Support
- Integrated GUI Support for MAJIC Series Intelligent JTAG Debug Probes
- Integrated Execution Tracing Window with Source Code Annotation
- Application Access to Host I/O System via EPI-OS facility
- Flash Programming Utilities & Sample Files

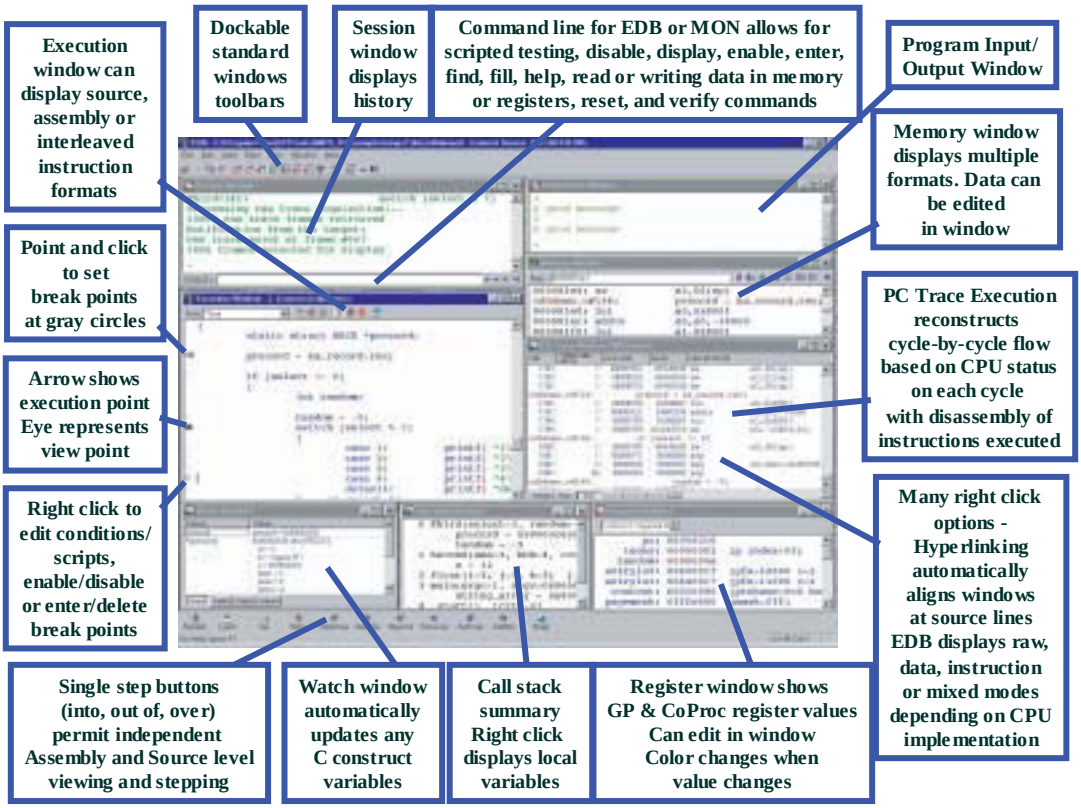


EDB features Integrated Trace Display

# MAJIC JTAG EMULATOR SERIES SELECTION GUIDE

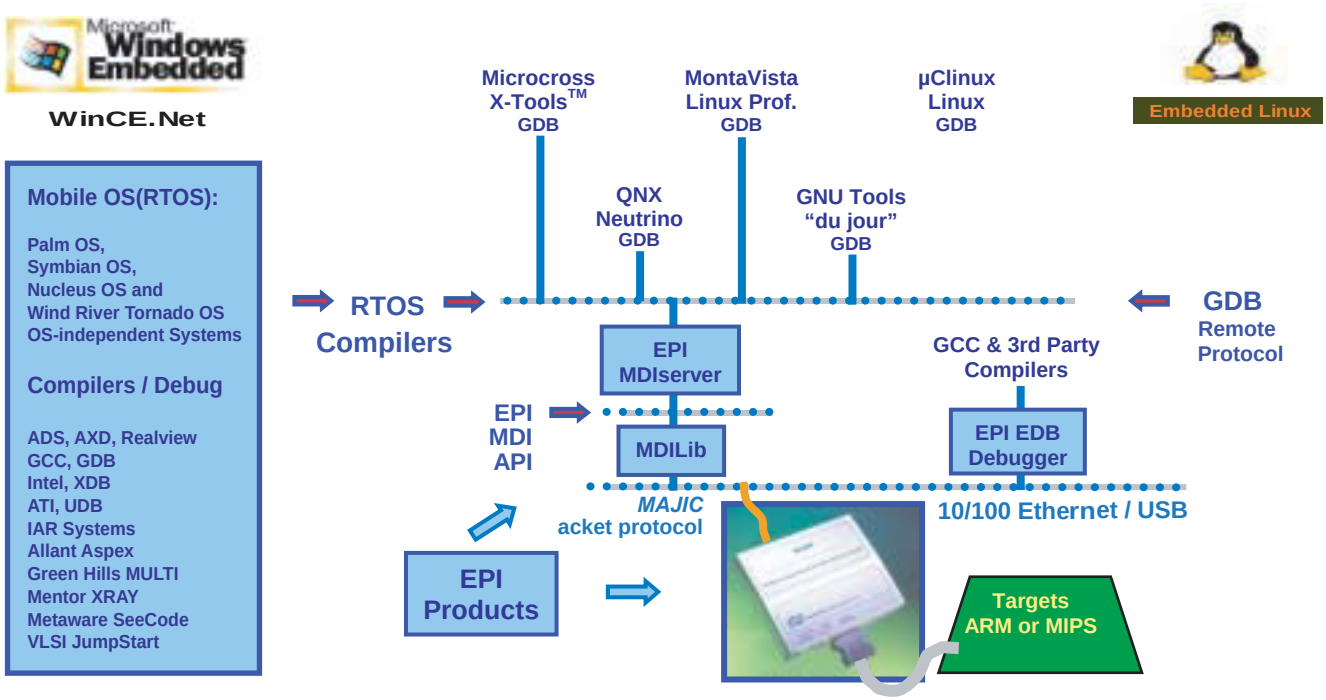
| | *MAJIC III* | *MAJIC II* | *MAJIC II MX* | *MAJIC II PLUS* |
|---|---|---|---|---|
| **Common Features** | • Non- intrusive, needs no target resources<br>• Ideal for SoC based applications<br>• Supports on-chip hardware breakpoints<br>• Unlimited software breakpoints<br>• ROMless booting<br>• Ethernet & Serial I/O Ports<br>• High speed download of application code<br>• Shared and remote operation<br>• Easy firmware updates via flash<br>• LEDs display operation status | | | |
| **Cores Supported** | • All ARM cores, Qualcomm, OMAP<br>• Broadcom 1100, 3310, 3310b, 3345, 3350, 3352, 3360, 6352, 7100<br>• IDT 32332, 32364, 32334, 32355<br>• Intel Xscale PXA250, PXA210, i80200, IOP310, IOP321, IXP425/2400/2800/2850, IXC1100, Bulverde<br>• Philips PR1900, PR1910, PR3940<br>• Lexra 4180, 4189, 4280, 4380, 5180, 5280, 8000<br>• LSI Logic 4102, 4103<br>• MTI 4kc, 4km, 4kp, 5kc<br>• Etc. | | | |
| **Other Differentiating Features** | • 10/100 base-T Ethernet / USB<br>• Supports ARM synthesizable cores<br>• Programmable JTAG clock (2kHz to 10 MHz)<br>• Supports sleep-mode<br>• Supports ARM RT clock<br>• Multi-TAP JTAG support<br>• Built-in memory test<br>• Concurrent debug mode<br>• Non-intrusive connect mode (most CPUs) | • 10/100 base-T Ethernet / serial<br>• Supports ARM synthesizable cores<br>• Programmable JTAG clock (2kHz to 40 MHz)<br>• Supports sleep-mode<br>• Supports ARM RT clock<br>• Multi-TAP JTAG support<br>• Built-in memory test<br>• Concurrent debug mode<br>• Non-intrusive connect mode<br>• (most CPUs)<br>Logic Analyzer connections (Trigger in/out) | • All the MAJIC II features, plus:<br>• Supports on-chip trace buffers<br>• MDS$^2$ technology<br>• Supports multi-cores debug<br>• Supports multiple architecture debug | • All the MAJIC II MX features, plus:<br>• ARM ETM/ Real Time Debug Trace Support<br>• EJTAG/PC Trace support<br>• External trace trigger<br>• External trace enable |
| **Debug Interface Protocol** | • Microsoft eXDI for Platform Builder in Windows CE<br>• ARM RDI<br>• Intel UDI for XDB-JTAG<br>• EPI MDI(includes GNU/GDB) | | | |
| **Compatible Debugger Software** | • ARM SDT, ADS, ADW, AXD, Real-View<br>• EPI CADB, CADB25<br>• EPI EDB<br>• EPI XDB-JTAG<br>• GNU GDB<br>• Green Hills MULTI<br>• Intel XDB-JTAG<br>• Mentor Graphics XRAY<br>• Metaware SeeCode<br>• Microsoft Platform Builder<br>• Wind River Tornado(opt 83mvx) | | | |

# EPI's Debug Environment



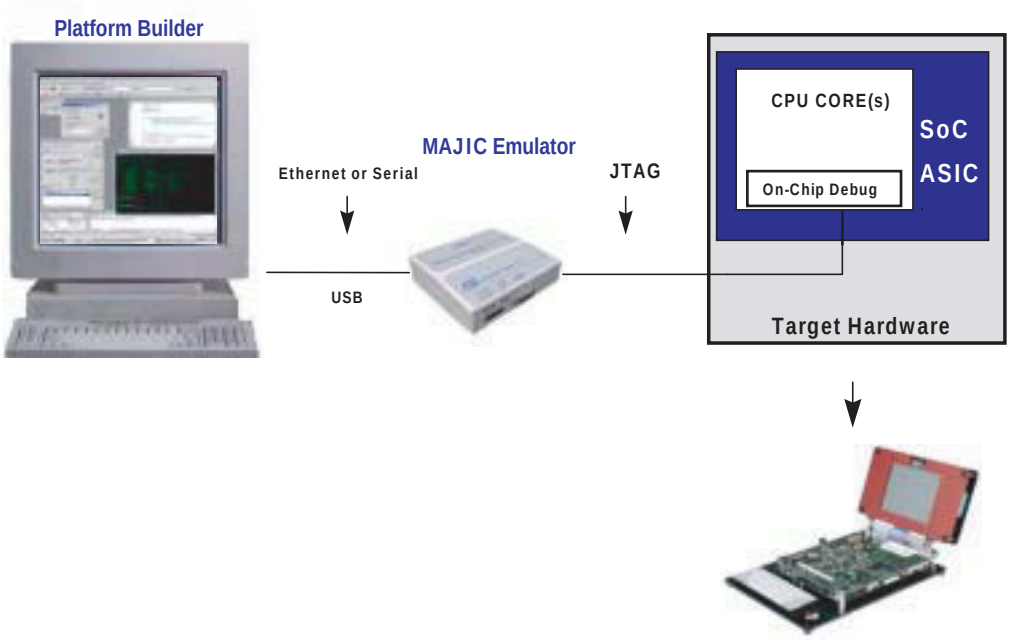

<EDB S/W 환경>

**EDB** EPI's debug interface libraries support hardware breakpoints for debugging BSP/driver code in ROM/Flash, and Flash memory programming utilities & sample Files.



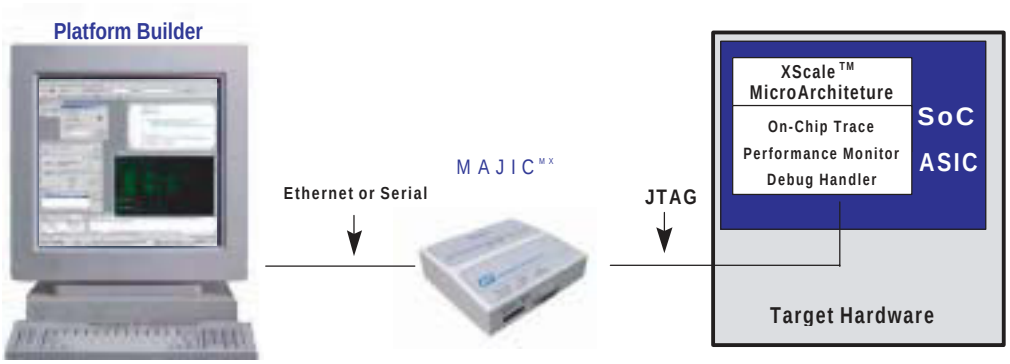

<MAJIC 지원 O/S 환경 및 구성>

# I. MAJIC Ddevelopment System



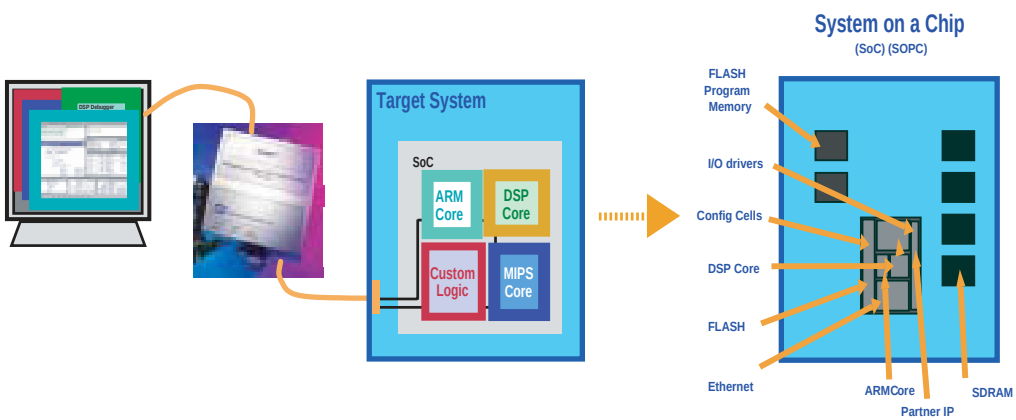


# II. MAJIC MX Ddevelopment System





# III. Multi debugging sessions



# MAJIC Supported Processors

| Source | Device Type | CPU/Core |
|---|---|---|
| ARM | 7TDMI Test Chip | 7TDMI |
| | Licensee ASIC/ASSP | ARM 7TDMI 7TDMI-S 720T 9TDMI 9E-S 920T 922T 926EJ-S 940T 946E-S 966E-S ARM7 or 9 as above(w/o RTCK)(Note1) ARM7 or 9 w/ETM |
| | ARM10 | ARM1020/1022E Etc. |
| Altera | EPXA1 EXPA4 EXPA10 | ARM 922T |
| Analog Devices | AD6489/6680/6681/6834/6843/6844/6846/6847 | Lexra 4180 & 4189 |
| ATI Technologies, inc | Xilleon220 /225 | MIPS 4Kc |
| Atmel | ATR0620 AT75C140/220/310 AT76C11x, 5xx AT78C1501 AT91F40816 AT91FR4081 AT91M4xxxx AT91M55800A AT91M63200 AT91R40807 | ARM 7TDMI |
| | AT91RM9200 | ARM 920T |
| Brecis | MSP2000/2005/2007/2100/3000/4000/5000 | MIPS |
| Broadcom | BCM1100/1101/3310/3310B/3345/3348/3350/3352/3360/4702 BCM4704/4710/5365/6345/6352/7100/7110/7115/7315/7320 | MIPS 3K MIPS4K |
| Conexant | CX84200 | ARM 7TDMI |
| | CN9414 CX22490/22492/22496/24430/24431/24943/24951/82100 CX82110/82310/82320/82340 | ARM 940T |
| | CX86111 | ARM 926EJ-S |
| Cirrus Logic | CS89712 EP7309/7311/7312/7339/9312 PS7500FE | MIPS |
| GlobespanVirata | Helium100/200/210-80 | ARM 7TDMI(x2) |
| | Helium500 | ARM 920T and 966E-S |
| IDT | RC32332/32333/32334/32336/32351/32355/32364/32365 | MIPS 32 Arch |
| | RC32438 | MIPS 4Kc |
| Intel | i80200(IOP310) i80321(IOP321) IXC1100 IXP420/421/422/425 IXP2400/2800/2850 PXA210/250/255/26x, Bulverde | Xscale(Note 3) |
| Ishoni Networks(Philips) | IBE-1000 PD2xxx PDT2000/2002/2102/2112/2114/2200/2210 PDT2402/4/8 PDT2412/4/8 | LX4180 LX4189 |
| Lexra | LX4180/4189/4280/4380/5180/5280 | Lexra |
| LSI Logic | EZ4102/4103 | MIPS Arch |
| Micronas | MDE-9500 | Lexra 4280 |
| MIPS Tech.Inc. | Licensee ASIC/ASSP(*=Pro series available) | MIPS32 Arch 4K(c,m,p) 4KE*(c,m,p) 4KSd* M4K* 5Kc 5Kf 24K |
| Motorola | MC9328MX1 | ARM 920T |
| | Creatalink2XT | |
| | MC9328MX21 | ARM 926EJ-S |
| NET Silicon | Net+ARM NS7520 | ARM 7TDMI |
| Oki | ML671K/674K/675K | ARM 7TDMI |
| Philips | SAF3100 | PR1900 |
| | PNX7850 | PR1910 |
| | ASSPs | PR1910 PR3940 |
| | RSP ASICs | ARM 7TDMI |
| | RSP ASICs ASICs | ARM 940T |
| PicoTurbo | | PT-100 PT-110 |
| Qualcomm | MSM3000/3300/5000/5010/5100/5105/5500/6000/6025/6050/6200 | ARM 7TDMI |
| | MSM6100/6250/6275/6300/6500/6700 | ARM 926EJ-S |
| Samsung | S3C4510B/20/30A S3F460H/441FX S3C44B0X/49F9X S5N8946/47 | ARM 7TDMI |
| | S3C2400/10/2440/24A0/2800 | ARM 920T |
| | S3C2500A/2501/2510 | ARM 940T |
| Sharp | LH75400/401/410/411 | ARM 7TDMI |
| | LH79520 | ARM 720T |
| | LH7A400/404 | ARM 922T |
| Texas Instruments (ARM) | TMS320c5470/1/2 TMS320DSC21 | ARM 7TDMI |
| | OMAP-310/1510/5910 | TI925 |
| | OMAP-710 | 7TDMI + TI925 |
| | OMAP-730/732 | 7TDMI + TI926TEJ |
| | OMAP-1610/1611/1612 | ARM 926TEJ |
| Texas Instruments(MIPS) | TNETC4310/20/4400/01 TNETD5301/5310/5320/7300 | MIPS32 4Kc MIPS32 4KEc |
| Triscend | TA7S20 | ARM 7TDMI |
| Zeevo | TC2000 | ARM 7TDMI |

# 임베디드 시스템 개발자 교육과정

(Xscale/ARM/AVR/8051/Bluetools)

## ■ 제공

-최적의 교육환경 마련

-최신설비와 현대적 교육운영

-다양한 실습 기자재

-준비된 최고의 강사진

-수료증 제공 및 동호회 구축

(주)마이크로비전

(주)마이크로비전 교육실

보드 및 교재

## ■ 교육일정

**임베디드 시스템 교육안내**

Xscale 개발자 교육 과정
WinCE.NET O/S 기반
매월 4째주 5일 과정
EBOOT 실습 보드(PXA25X)제공

ARM 개발자 교육 과정
매월 3째주 4일 과정
BW-3SC44B0X 보드 무상 제공

MAJIC 에뮬레이터 무료 교육
(ARM / Xscale / MIPS)
매월 1 째주 토요일
h/w 셋팅 / 플래시 다운로딩

AVR/8051 개발자 교육 과정
매월 2째주 2일 과정

Bluetooth 개발자 교육 과정
분기별 2일 과정
BlueBoard 2EA 무상 제공

**무료 기술 교육 안내**

**기술지원정보교환의장소**

| 교육과정명 | 주 요 내 용 | 기타 / 특전 |
|---|---|---|
| Xscale 프로세서<br>(월 1회 5일간)<br>유료 | -Xscale의 구조/이해<br>-Xscale 기반 WinCE.Net O/S 교육<br>-Xscale 기반 임베디드 리눅스 O/S 교육<br>-디바이스 Driver 설계 및 실습 | -Xscale 응용보드 실습<br>-교육후 실습보드 증정<br>-교육 수료증 제공 |
| ARM 프로세서 교육<br>(월 1회 4일간)<br>유료 | -ARM의 구조/이해<br>-개발환경 구축, CPU Boot<br>-H/W, 펌웨어 설계 과정<br>-소스라인 디버깅 방법 실습 | -ARM 응용보드 실습<br>-교육후 실습보드 증정<br>-교육 수료증 제공 |
| AVR / 8051 프로세서<br>(월 1회 3일간)<br>유료 | -AVR의 구조/이해<br>-AVR 프로그래밍 기법<br>-AVR 개발환경 구축 및 실습<br>-Ethernet 원격제어 응용 및 실습 | -AVR 응용보드 실습<br>-교육후 실습보드 판매<br>-교육 수료증 제공 |
| Bluetools 교육<br>(분기 1회 2일간)<br>유료 | -블루투스 하드웨어 구조<br>-프로토콜스택, 프로파일 이해<br>-인증절차 및 안테나 교육<br>-실제제품 실습 과정 병행 | -블루트수 타겟보드 실습<br>-교육후 실습보드 증정<br>-교육 수료증 제공 |
| ARM / Xscale<br>AVR / 8051<br>(월 1회 4시간)<br>무료 | -각 제품 장비 운용및 사용법<br>-임베디드 시스템 장비 소개 | -카다로그 제공<br>-교재 제공 |

교육일정은 상황에 따라 다소 변경될수 있습니다. 자세한 교육 내용은 www.microvision.co.kr 참조.

Micro Vision (주)마이크로비전

# 기술 지원 / 정기 교육...

## ■ 기술지원

I. MAJIC 에뮬레이터 정기 무료 교육

II. H/W 셋팅, 플래시 다운로딩 지원

III. Bootload 기술지원 / 개발 용역 대행

## ■ 교육 프로그램

### I. 무료 기술 교육 과정 (MAJIC JTAG Emulator)

| 교육대상 | 교육목적 | 교육내용 | 교육교재 | 강사 |
|---|---|---|---|---|
| - EPI MAJIC 사용자<br>- 구매 희망자 | - ARM 개발자들의 개발 환경 구축 시간 절약 및 하드웨어 디버깅에 관한 이해와 실습<br>- CPU, MEMORY 및 주변 I/O 장치 테스트<br>- JTAG 에뮬레이터를 이용한 하드웨어 디버깅 방법<br>- ARM 개발자들의 개발환경 구축과정 및 환경에 대한 자료 제공 | - EPI MAJIC 설치 및 사용법<br>- Hardware Debugging 및 F/W Debugging<br>- EDB 및 Monice 사용법<br>- Flash programming | - How to use MAJIC (한글메뉴얼)<br>- Hardware Debugging for ARM | - (주)Microvision TS (Technical Support) 팀<br>- 매월 강의 (1일간) |

### II. Xscale 개발자 교육과정 (5일 과정)

| | 1일차 | 2일차 | 3일차 | 4일차 | 5일차 |
|---|---|---|---|---|---|
| 10:00 ~ 11:00 | Windows CE.NET Features & Architecture | Embedded System의 개요 | 펌웨어 설계, Processor 비교 XScale Architecture | USB 개요, USB Transfers | WindowsCE.NET USB Driver 분석 |
| 11:00 ~ 12:00 | Platform Builder 사용법 Build Process의 이해 | 범용 CPU 및 CPU 관련 | Xscale Instruction PXA25X 분석 및 실험이해 | Control, Bulk, Interrupt, Isochronous Transfer이해 | 응용 프로그램 실습 |
| 점 심 | | | | | |
| 13:00 ~ 14:00 | Platform Builder 실습 | 제품 설계 타겟 제품 디자인 고려사항 | WinCE.NET 구조 분석 및 개발 방법 실습 | USB Controller의 소개, Interface, 구조 | IAR ARM 컴파일러 구조 설명 |
| 14:00 ~ 15:00 | Debugging Windows CE.NET Debug Zone , JIT Debugging | 블록도 설명<br>회로도 작성<br>메모리 맵 설정 | WinCE.NET 에서의 EBOOT 구조 분석 및 개발 방법 습득 | 개발보드 Schematic 설명<br>Controller 내부 구조 | 컴파일러에서의 시작 프로그램 설명 |
| 15:00 ~ 16:00 | Debugging 실습 | 개발툴 사용 방법 및 실험<br>JTAG 분석 및 실험 | WinCE.NET 4.2에서 BSP 수정 및 실습 및 설명 | Enumeration, Descriptor 설명 | 모니터 프로그램 포팅 |
| 16:00 ~ 17:00 | | MAJIC tool 사용법 및 설명 | | Enumeration 순서<br>Packet 분석 | JTAG 디버거로 관련 프로그램 실습 |

1. 교육과정 : XScale / WinCE.Net
2. 교육대상 :
   -XScale/ARM CPU 관련 H/W, S/W 개발자
   -WinCE.Net 관련 개발자
   -EBOOT및 포팅에 관심이 있는 개발자
3. 교육특징 : 1인 1PC의 실습교육
4. 교육인원 : 15명
5. 교육비용 : 유료
6. 제공사항:
   -실습용 Application 보드 제공 (PXA25X=XScale)
   -JTAG Debugger 툴 교육수료후 무료제공
   -EBOOT, BSP, Monitor 프로그램 및 사용자 프로그램 예제

*기타 자세한 내용이나 문의는 연락바람

### III. ARM 개발자 교육과정 (4일 과정)

| | 1일차 | 2일차 | 3일차 | 4일차 |
|---|---|---|---|---|
| 10:00 ~ 11:00 | Embedded System개요 | HARDWARE 개 발 개 요 | 보드 Source 설명 | HARDWARE /SOFTWARE 개발절차 |
| 11:00 ~ 12:00 | ARM Core Architectur | Compiler 이해/활용 | | JTAG개요 |
| 점 심 | | | | |
| 13:00 ~ 14:00 | ARM Core 응용I/ 44b0 CPU 소개 | EMBEDDED C언어 입문 | CPU 내장 기능 소프트웨어 테스트I 실습 | MAGIC 소개 및 사용법 시연 |
| 14:00 ~ 15:00 | 보드사용법 | 보드 BOOTLOAD 설명 | | JTAG DEBUGGER 사용실습 |
| 15:00 ~ 16:00 | 개발환경구축 | 보드 자원관리 IRQ/MEMORY 관리 | CPU 내장 기능 소프트웨어 테스트II 실습 | |
| 16:00 ~ 17:00 | 보드 기본 사용법 | FLASH Memory 관리방법 | | CPLD & LCD KIT 사용입문 |

1. 교육과정 : ARM7
2. 교육대상 :
   -ARM CPU관련 H/W, S/W 개발자,
   -ARM CPU관련 Non-OS base의 시스템을 개발하려고 하는 사람
3. 교육특징 : 1인 1PC의 실습교육
4. 교육인원 : 15명
5. 교육비용 : 유료
6. 제공사항:
   -실습용 application 보드 제공 (BW-S3C44BOX=ARM7TDMI),
   -JTAG Debugger 툴 교육수료후 무료제공
   -BOX, 소스프로그램 CD
   -케이블, 아답타
   - 교재 : 강사 저작
   - Emulator : Magic Debugger tool
   - IAR社 ARM 컴파일러 S/W 30days evaluation 제공

*기타 자세한 내용이나 문의는 연락바람

*교육일정은 상황에 따라 다소 변경될수 있습니다. 자세한 교육 내용은 www.microvision.co.kr 참조.

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# 무료 교육 강좌

## MAJIC JTAG Emulator

### 목 적

본 교육과정은 XScale/ARM 개발자들의 개발 환경 구축 시간 절약 및 하드웨어 디버깅에 관한 이해와 실습을 통한 기본 기술을 익히기 위한 과정입니다.
하드웨어 엔지니어들이 보드가 처음 나오면 CPU, MEMORY 및 주변 I/O 장치들의 테스트가 필수적입니다.
JTAG 에뮬레이터를 이용하여 하드웨어 디버깅 방법을 교육합니다.
또한, ARM 개발자들의 개발환경 구축과정에 대한 전반적인 개발환경에 대한 자료를 제공합니다.

### 교육대상

- EPI MAJIC 사용자
- 구매 희망자

### 교육 일정 ( 매월 강의 )

- 날 짜 : 매월 토요일 1일간
- 시 간 : 10:00 ~

### 강사

- (주)Microvision TS (Technical Support) 팀
  참고자료 (교육시 교재는 제공되지 않습니다.)
- How to use MAJIC (한글메뉴얼)
- Hardware Debugging for XScale / ARM

### 강의내용

- EPI MAJIC 설치 및 사용법
- Hardware Debugging 및 F/W Debugging
- EDB 및 Monice 사용법
- Flash programming

### 접수방법

- 교육 신청 방법 :
  MAJIC 교육 신청서 작성후 이메일 송부
- 선착순 13명 마감
  E-mail로 문의 하시기 바랍니다.
- 교육신청 및 일정 관련 문의 : 서영진 대리
  TEL : 02)3283-0101 FAX : 02)3283-0160
  URL :www.microvision.co.kr
  E-mail:epi@microvision.co.kr
  * 교육을 희망하시는 분은 교육 참가 신청서를 이메일로만 신청하여 주시기 바랍니다.

### 교육 연기 및 취소

- 교육 연기 및 취소는 반드시 교육 시작 3일전까지 연락 주시기 바랍니다.
  또한, 교육사정상 교육이 연기되거나 취소되는 경우엔 사전 통보해드립니다.

### 교육 장소

- 교육장소 및 위치 : 마이크로비젼 교육장

# IAR Embedded Workbench™ for ARM


*The IAR Embedded Workbench is a set of highly sophisticated and easy-to-use development tools for programming embedded applications. It integrates the IAR C/EC++ compiler, assembler, linker, librarian, text editor, project manager and C-SPY debugger in one integrated development environment (IDE). With its built-in chip-specific optimizer, the IAR Embedded Workbench for ARM generates very efficient and reliable FLASH/PROMable code for the ARM7™, ARM9™, ARM9E™, ARM10™ and Intel® XScale™ families. C-SPY—IAR Systems' state-of-the-art high-level language debugger—supports the ARM Multi-ICE JTAG interface and other RDI-based JTAG interfaces, Macraigor's Raven and Wiggler JTAG interfaces as well as ARM Angel. It also includes a CMX-RTX RTOS plug-in module. In addition to solid technology, IAR also provides professional world-wide technical support.*

## HIGHLIGHTS

- New project manager with text-based project files
- Sample projects included
- Support for the VFP9-S floating-point co-processor
- C-SPY RTOS plug-in module for Express Logic's ThreadX included
- C-SPY support for Macraigor's mpDemon
- EPI JEENI driver now supports Ethernet connectivity

## INTEGRATED DEVELOPMENT ENVIRONMENT (IDE) WITH NEW PROJECT MANAGER

- A modular and extensible IDE running under Windows 98/ME/NT4/2000/XP
- Support for ARM7™, ARM9™, ARM9E™, ARM10™, and Intel® XScale™. For detailed information about the supported cores, see www.iar.com
- A modular and extensible IDE running under Windows 98/ME/NT4/2000/XP
- Create projects, edit files, compile, assemble, link and debug your applications within the seamlessly integrated environment
- Tool options configurable on global, group of source files, or individual source files level
- Multiple projects in the same workspace
- Hierarchical project representation shows all different source and output files and gives an overview of their settings
- XML-based project files
- Easy to integrate external tools in the build process
- Multi-byte editor

## COMPILER

- ISO/ANSI standard C and Embedded C++ Compiler
- Each function can be compiled in ARM or Thumb mode
- Multiple levels of optimizations for code size and execution speed
- Extended ARM-specific keywords
- Built-in advanced ARM-specific optimizer
- Reentrant code
- Support for VFP9-S (see highlights)
- Extended support for EC++ including templates, namespaces, mutable specifier, static cast, reinterpret cast and const cast
- Easy and fast interrupt handling directly in C/EC++
- Mixed C/EC++ and assembler listings
- Multibyte character support

## IAR C-SPY DEBUGGER

- Complex code and data breakpoints
- C/EC++ call stack with parameters
- Complete support for stack unwinding even at high optimization levels
- I/O and interrupt simulation
- Versatile monitoring of registers, structures, call chain, locals, global variables and peripheral registers
- Fine-grain single stepping
- Profiling and code coverage
- Target access to host file system via file I/O
- Continuous tracing and logging of arbitrary C-SPY expressions such as variables and register values
- I/O register definition files for different ARM chips
- ARM Angel debug monitor support
- CMX-RTX RTOS plug-in module included
- ThreadX RTOS plug-in module included
- Compatibility with µC/OS-II RTOS; plug-in module available from Micrium

## IAR C-SPY JTAG INTERFACE

- Real-time execution
- ARM Multi-ICE JTAG interface and other RDI-based JTAG interfaces
- Verified with EPI MAJIC, MAJIX-MX, MAJIC-PLUS, Abatron BDI1000/BDI2000, Aiji OPENice32-A900, Ashling OPELLA and Signum JTAGjet-ARM
- Macraigor mpDemon, Raven and Wiggler JTAG interfaces
- EPI Jeeni JTAG interface

## ASSEMBLER

- A powerful relocating macro assembler with a versatile set of directives and operators
- Built-in C language preprocessor, accepting all C macro definitions

IAR SYSTEMS
From Idea To Target

www.iar.com