Application Note
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MAJIC Support for Hardware Emulation Systems

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Introduction

Many ASIC design teams use a hardware emulation system for functional validation prior to committing their design to silicon. Increasing the test coverage in the emulation environment reduces the risk that a serious design defect will go unnoticed until too late, so for System-on-Chip (SoC) designs that incorporate a CPU it is desirable to validate the JTAG interface and its connection to the processor's debug support unit. It is also desirable to stimulate the hardware design using actual device driver software, which may itself need to be debugged.

The best way to accomplish these goals is to connect an actual MAJIC to the hardware emulator so that it can interact with the emulation model. This application note explains the special considerations that arise when using a MAJIC in this type of environment.

Note: Chapter 3 of the *MAJIC User's Manual* presents complete information on the MAJIC Setup Wizard and user defined configuration files, which are mentioned in this application note.

Getting Support

If you have additional questions on this or another topic, please do not hesitate to contact our technical support staff. We are committed to making sure the MAJIC development environment works well for you.

How Slow Can You Go?

The fundamental problem in using MAJIC with a hardware emulator is that the emulated processor operates much slower than the real processor eventually will. This implies that the JTAG interface must also work much slower than normal, because there is usually some restriction on the ratio of the JTAG clock to the system clock. Please check with your processor vendor to confirm their specific requirements, but in general it is best to make sure the JTAG clock is slower than the system clock.

Hardware emulation systems typically operate at much less than 1MHz, so MAJIC must be configured to ensure that the JTAG clock will be slow enough for your emulation environment. The JTAG engine built into MAJIC is optimized for high speed operation, so the way to achieve very slow JTAG clock rates is to disable the JTAG engine and select the built-in software driver instead. This may be accomplished by setting the **`Ice_Jtag_Clock_Freq`** option to zero, by creating your own start-up file using the MAJIC Setup Wizard.

But even the software driver normally operates too fast for some hardware emulation systems. The software JTAG driver manually operates the JTAG signals when called upon to perform a JTAG scan operation, so the effective clock rate of the JTAG interface varies depending on what MAJIC is trying to do. A peak rate may exceed 250kHz. To ensure that peak rate does not exceed the maximum frequency supported by your hardware emulation system, the **`Ice_Jtag_Clock_Delay`** option can be set to specify the minimum pulse width of the JTAG clock, in microseconds. The setting applies to both the high phase and low phase of the clock, so a setting of 5 guarantees a maximum peak frequency of 1/(5+5)µs = 100kHz.

Note: The **`Ice_Jtag_Clock_Delay`** option is only in effect if **`Ice_Jtag_Clock_Freq`** is set to **`0`**.

The MAJIC Setup Wizard does not directly support the **Ice_Jtag_Clock_Delay** option because most users never need to worry about it. However, you can create a command file as follows, and select that as the user supplied initialization file in the wizard. It is important to set all the JTAG options before MAJIC attempts to initialize the JTAG interface, so you should select **OFF** for **Ice_Power_Sense** in the MAJIC Setup Wizard, and then set **Ice_Power_Sense** as appropriate for your design in the user supplied initialization file.

```
eo Ice_Jtag_Clock_Freq = 0    // Select software JTAG driver
eo Ice_Jtag_Clock_Delay = ___ // Fill in the blank with your setting in µs
eo Ice_Power_Sense = _____    // VREF, RST, or TRST, depending on your H/W
```

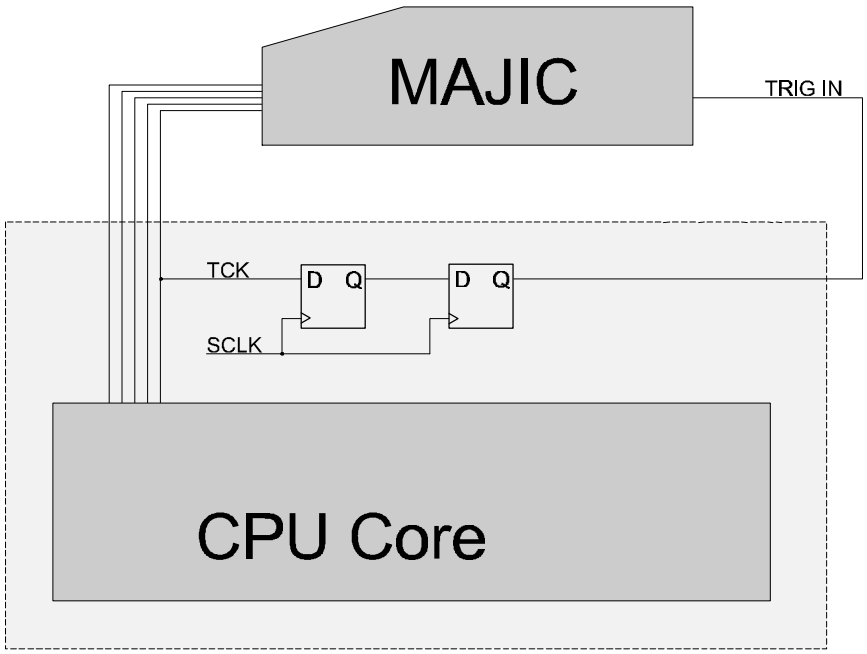
Software Time-Outs

Using a very slow JTAG clock means that JTAG operations take much longer to complete than they normally would. Since any given debug service request may require a number of JTAG operations, the delays arising from the slow JTAG clock are compounded. This may cause problems in debug environments which implement a software time-out on debug service requests issued to the MAJIC probe. When using an EPI debugger, MAJIC has the ability to update the debugger on its progress and thereby reset the software timer; apart from being slow everything works normally. However, there is no mechanism for this when using third party debuggers, so a third party debugger may experience software time-outs that do not occur with EPI debuggers.

Synchronized JTAG Operation

One big advantage to using a hardware emulation system is that you can stop the model at critical points and inspect its state. When this happens, the processor clock effectively stops, so the JTAG clock must stop too or the processor's JTAG interface will lose synchronization with MAJIC. Furthermore, many emulation systems use a variable clock rate; the more work it has to do in a given emulation clock cycle the longer that cycle takes in real time. Since the maximum JTAG clock must be below some threshold derived from the minimum system clock, the JTAG clock will be much slower than would otherwise be necessary during times when the emulation clock is above its minimum.

A better solution is to allow the hardware emulation system to dynamically throttle the JTAG clock rate. MAJIC supports this by monitoring a copy of the JTAG clock signal that has been synchronized to the system clock by a circuit within the hardware emulation environment. For ARM processors which support the RTCLK signal, that signal automatically throttles MAJIC's JTAG clock, so there is nothing special to do. For other processor implementations, EPI recommends synchronizing the JTAG clock within the hardware emulation model and connecting the result to MAJIC's trigger input, as shown below.



To use the trigger input this way, the **Ice_Trigger_In** option must be set to select **JTAG_SYNC** mode. The MAJIC Setup Wizard does not directly support this option because most users never need to worry about it. However, you can create a command file as shown below and select that as a user supplied initialization file in the wizard. It is important to set all the JTAG options before MAJIC attempts to initialize the JTAG interface, so you should select **OFF** for **Ice_Power_Sense** in the MAJIC Setup Wizard, and then set **Ice_Power_Sense** as appropriate for your design in the user supplied initialization file.

```
eo Ice_Jtag_Clock_Freq = 0    // Select software JTAG driver
eo Ice_Trigger_In = JTAG_SYNC  // Use trigger input BNC to sync JTAG clock
eo Ice_Power_Sense = _____     // VREF, RST, or TRST, depending on your H/W
```

Notes: You may use both **Ice_Jtag_Clock_Delay** and **Ice_Trigger_In** at the same time to control the peak JTAG clock rate and freeze the JTAG clock when the emulation model stops. The semantics are that it waits until the synchronized clock is received and the specified time has elapsed. Just remember to set both before **Ice_Power_Sense**.

JTAG_SYNC mode is only supported when **Ice_Jtag_Clock_Freq** is set to **0**. The RTCLK signal provided by certain ARM cores is supported regardless of **Ice_Jtag_Clock_Freq**, but if the processor's system clock is below 8MHz then setting **Ice_Jtag_Clock_Freq** to **0** is recommended.