Application Note
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MAJIC® Interface Specifications for ARM Debug Interface and Intel XScale® Technology

0380-0188-10 Rev 2.2

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Introduction

This application note provides technical specifications for the MAJIC® Series of Intelligent Debug Probes when used with ARM7 or ARM9 processors that include the ARM Debug Macrocell, or with processors based on Intel XScale® technology.

- Cabling options.
- Debug connector details: pin-outs and recommended part numbers.
- Board design considerations.
- Electrical specifications for each model in the MAJIC® Series of Intelligent Debug Probes.

Cable Kit Options

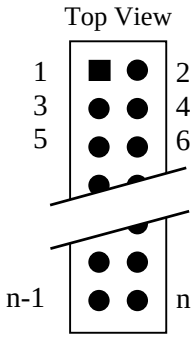
There are several cable kit options available for the MAJIC® Series, and it is important to choose the right cable kit(s) for your target board(s) and MAJIC® model. The following table shows the most commonly used cable kits for target boards incorporating an ARM core or Intel XScale® core. Details on the connectors' pin-outs, and recommended board design practices follow on the next few pages.

Target Connector	**MAJIC (I, II, or III)** **MAJIC^{MX} (I, II)** **MAJICO**	**MAJIC^{PLUS}**	**MAJIC^{PLUS}/II**
12-Pin Fine Pitch JTAG	CK-FPJ12	CKP-FPJ12	CKP2-FPJ12
14-Pin JTAG, Texas Instruments pin assignment	CK-TX14	Not Supported	CKP2-TX14
14-Pin JTAG, ARM pin assignment	CK-ARM14	CKP-ARM14	CKP2-ARM14
20-Pin JTAG, ARM pin assignment	CK-ARM20	CKP-ARM20	CKP2-ARM20
20-Pin JTAG, ARM pin-out and **separate** 38-Pin Mictor for ETM	CK-ARM20	CKP-ARM38 –or– AP-ARM38+20	AP2-ARM38+20
38-Pin Mictor, combined JTAG and ETM	CK-ARM38	CKP-ARM38 –or– AP-ARM38/A	AP2-ARM38/A

Notes:

- The CK-01AM kit includes both CK-ARM14 and CK-ARM20.
- The CKP-01AM kit includes CKP-ARM14, CKP-ARM20, and CKP-ARM38.
- For demultiplexed ETM trace support, where the target provides two Mictor connectors, a MAJIC$^{PLUS®}$/II probe with two AP2-ARM38/A cable kits is required.

JTAG Headers



Notes:

- The ARM14 and FPJ12 connectors are **not** suitable for ARM processors that require the RTCLK signal.
- Technical details on the JTAG signals are discussed in the *Board Design Considerations* and *Electrical Specifications* sections of this application note.
- See page 4 for recommended connector vendor part numbers.

Pin	ARM 20-Pin 2x10 0.10"		ARM 14-Pin 2x7 0.10"		TX 14-Pin 2x7 0.10"		FPJ 12-Pin 2x6 0.05"	
1	VTRef	10k pull-up	VTRef	10k pull-up	TMS	10k pull-up	nTRST	10k pull-up
2	VSupply	(not used)	GND		nTRST	10k pull-up	GND	
3	nTRST	10k pull-up	nTRST	10k pull-up	TDI	10k pull-up	TDI	10k pull-up
4	GND		GND		GND		GND	
5	TDI	10k pull-up	TDI	10k pull-up	VTref	10k pull-up	TDO	33 Ω series
6	GND		GND		n/c		GND	
7	TMS	10k pull-up	TMS	10k pull-up	TDO	33 Ω series	TMS	10k pull-up
8	GND		GND		GND		GND	
9	TCK	10k pull-up	TCK	10k pull-up	RTCK	33 Ω series	TCK	10k pull-up
10	GND		GND		GND		GND	
11	RTCK	33 Ω series	TDO	33 Ω series	TCK	10k pull-up	nSRST	10k pull-up
12	GND		nSRST	10k pull-up	GND		GND	
13	TDO	33 Ω series	VTRef	10k pull-up	nEMU0	(not used)		
14	GND		GND		nEMU1	(not used)		
15	nSRST	10k pull-up						
16	GND							
17	DBGRQ	10k pull-down (not used)						
18	GND							
19	DBGACK	10k pull-down (not used)						
20	GND							

38-Pin Mictor Connectors

Pin	Single Target		Dual Target		Multiplexed Target	
1	n/c		n/c		n/c	
2	n/c		n/c		n/c	
3	n/c		n/c		n/c	
4	n/c		n/c		n/c	
5	GND		TRACECLK_B	33 Ω series	GND	
6	TRACECLK	33 Ω series	TRACECLK_A	33 Ω series	TRACECLK	33 Ω series
7	DBGRQ	10k pull-down	DBGRQ	10k pull-down	DBGRQ	10k pull-down
8	DBGACK	10k pull-down	DBGACK	10k pull-down	DBGACK	10k pull-down
9	nSRST	10k pull-up	nSRST	10k pull-up	nSRST	10k pull-up
10	EXTTRIG	10k pull-up	EXTTRIG	10k pull-up	EXTTRIG	10k pull-up
11	TDO	33 Ω series	TDO	33 Ω series	TDO	33 Ω series
12	VTRef	10k pull-up	VTRef	10k pull-up	VTRef	10k pull-up
13	RTCK	33 Ω series	RTCK	33 Ω series	RTCK	33 Ω series
14	VSupply	(not used)	VSupply	(not used)	VSupply	(not used)
15	TCK	10k pull-up	TCK	10k pull-up	TCK	10k pull-up
16	TRACEPKT[7]	33 Ω series	TRACEPKT_A[7]	33 Ω series	n/c	10k pull-up
17	TMS	10k pull-up	TMS	10k pull-up	TMS	10k pull-up
18	TRACEPKT[6]	33 Ω series	TRACEPKT_A[6]	33 Ω series	n/c	10k pull-up
19	TDI	10k pull-up	TDI	10k pull-up	TDI	10k pull-up
20	TRACEPKT[5]	33 Ω series	TRACEPKT_A[5]	33 Ω series	TRACEPKT[14] TRACEPKT[15]	33 Ω series
21	nTRST	10k pull-up	nTRST	10k pull-up	nTRST	10k pull-up
22	TRACEPKT[4]	33 Ω series	TRACEPKT_A[4]	33 Ω series	TRACEPKT[12] TRACEPKT[13]	33 Ω series
23	TRACEPKT[15]	33 Ω series	TRACEPKT_B[3]	33 Ω series		
24	TRACEPKT[3]	33 Ω series	TRACEPKT_A[3]	33 Ω series	TRACEPKT[10] TRACEPKT[11]	33 Ω series
25	TRACEPKT[14]	33 Ω series	TRACEPKT_B[2]	33 Ω series		
26	TRACEPKT[2]	33 Ω series	TRACEPKT_A[2]	33 Ω series	TRACEPKT[8] TRACEPKT[9]	33 Ω series
27	TRACEPKT[13]	33 Ω series	TRACEPKT_B[1]	33 Ω series		
28	TRACEPKT[1]	33 Ω series	TRACEPKT_A[1]	33 Ω series	TRACEPKT[6] TRACEPKT[7]	33 Ω series
29	TRACEPKT[12]	33 Ω series	TRACEPKT_B[0]	33 Ω series		
30	TRACEPKT[0]	33 Ω series	TRACEPKT_A[0]	33 Ω series	TRACEPKT[4] TRACEPKT[5]	33 Ω series
31	TRACEPKT[11]	33 Ω series	TRACESYNC_B	33 Ω series		
32	TRACESYNC	33 Ω series	TRACESYNC_A	33 Ω series	TRACEPKT[0] TRACEPKT[3]	33 Ω series
33	TRACEPKT[10]	33 Ω series	PIPESTAT_B[2]	33 Ω series		
34	PIPESTAT[2]	33 Ω series	PIPESTAT_A[2]	33 Ω series	PIPESTAT[2] TRACEPKT[2]	33 Ω series
35	TRACEPKT[9]	33 Ω series	PIPESTAT_B[1]	33 Ω series		
36	PIPESTAT[1]	33 Ω series	PIPESTAT_A[1]	33 Ω series	PIPESTAT[1] TRACEPKT[1]	33 Ω series
37	TRACEPKT[8]	33 Ω series	PIPESTAT_B[0]	33 Ω series		
38	PIPESTAT[0]	33 Ω series	PIPESTAT_A[0]	33 Ω series	PIPESTAT[0] TRACESYNC	33 Ω series

Mictor Notes:

1. DBGACK is only used when tracing with the MAJIC$^{PLUS®}$ passive probe (CKP-ARM38). DBGACK is ignored when using any of the active probes (AP-xxx or AP2-xxx), and when tracing is disabled. DBGREQ is never used.
2. MAJIC$^{PLUS®}$/I with a CKP passive probe, and MAJIC$^{PLUS®}$/II with an AP2 active probe support full trace width. MAJIC$^{PLUS®}$/I with an AP active probe, however, supports a maximum of 8 TRACEPKT bits.
3. Demultiplexed 4-bit tracing uses the same connector pinout as the Dual Target connector. Demultiplexed 8-bit and 16-bit tracing use two Mictor connectors both with the Single Target pinout, but with the JTAG signals connected only on the primary connector. MAJIC$^{PLUS®}$/II is required to support demultiplexed tracing.
4. Port B in the dual ETM configuration is not presently supported. Please contact our sales department if you foresee a need for this capability.
5. Multiplexed trace mode is not presently supported. Please contact our sales department if you foresee a need for this capability.

Note: Refer to the *MAJIC$^{PLUS®}$ Support for ARM/ETM* application note for additional information on using a MAJIC$^{PLUS®}$ probe with ARM/ETM, and technical details of each MAJIC$^{PLUS®}$ hardware configuraiton.

Debug Connector Part Numbers

Connector	Part Number	Description
12-pin, fine pitch header	Samtec FTSH-106-01-F-DV-A	Dual row (2x6), 0.05 inch spacing, surface mount header
14-pin header	3M 2414-600UB	Dual row (2x7), 0.1 inch spacing, surface mount header
20-pin header	3M 2520-6002UB	Dual row (2x10), 0.1 inch spacing, surface mount header
38-pin Mictor	AMP 2-767004-2	Vertical, surface mount, board to board/cable connector
38-pin Mictor	AMP 767054-1	Vertical, surface mount, board to board/cable connector
38-pin Mictor	AMP 767061-1	Vertical, surface mount, board to board/cable connector
38-pin Mictor	AMP 767044-1	Right Angle, straddle mount, board to board/cable connector

Note: Refer to connector vendor's technical documentation for dimensions and other PCB layout details.

Board Design Considerations

This section provides additional information on board design considerations that arise when designing a target board which incorporates an ARM core or Intel XScale® core.

Reset Management

- The nSRST (system reset) signal should be connected so that the target system (including the CPU) will be reset when it is asserted (low) by the MAJIC®, but will not result in nTRST (JTAG reset) being asserted on the target processor. This is recommended for ARM targets, and required for full support with Intel XScale® cores.
- The nSRST signal is an open-collector signal, so you must provide a pull-up for this signal. It may be tied directly to the reset switch or power-up reset circuit on your board.

JTAG Interface

- Some CPU data sheets recommend a pull-down on certain JTAG signals instead of a pull-up. The MAJIC® probe can support that recommendation, but the signals should not be left floating.
- Not all CPU variants provide an RTCK signal. If your CPU does not have this signal, then the RTCK pin on the debug connector should be grounded or pulled up with a 10k resistor. EPI strongly recommends against connecting TCK directly to RTCK, as this effectively doubles the length of the TCK signal, and puts your CPU in the middle of the TCK net.
- If you have more than one processor that supports RTCK, then RTCK from the processor with the slowest system clock should be used. Alternatively, you can daisy chain RTCK from one device to TCK of the next device, following the same path as TDO-TDI. The best solution, however, is to combine the RTCK signal from all of the cores into one RTCK signal that is presented to the MAJIC® probe. Please contact EPI technical support for additional information.

PCB Layout

- Avoid placing any tall components near the debug connector, and locate it in a way that is easy to reach (near the edge of the board). We recommend clearly labeling the debug connector and the position of pin 1 on the PCB.
- If you have more than one JTAG device on the scan chain, then the debug connector should be at the end of the JTAG nets, not in the center of the nets (i.e. the JTAG signals must not fan out from the debug connector to multiple devices). Please refer to the *MAJIC® Support for Multi-TAP JTAG Configurations* application note (P/N 0380-0243-10) for additional information.
- It is important to keep the trace signals short, and even more important to make them equal in length. The 33 Ω series termination resistors should be placed as close as possible to their respective processor pins. If the trace pins can be reconfigured for alternate signals, you should provide a build option to disconnect their alternate function.
- All unused trace pins should be grounded or pulled up.

Electrical Characteristics

This section provides the JTAG and ETM electrical characteristics for each model in the MAJIC® Series of Intelligent Debug Probes.

JTAG Interface for MAJIC®/I Series

DC Characteristics	Note	Specification
Target I/O Voltage		1.65V (1.8V nominal) to 3.5V CMOS 3.3V or 5V TTL
Output Drive: TCK		± 6mA at 1.8V ± 12mA at 2.5V ± 18mA at 3.3V
Output Drive: nTRST, TMS, TDI		± 4mA at 1.8V ± 6mA at 2.5V ± 8mA at 3.3V
Output Drive: nSRST	1.1	+3mA/-40µA at 1.8V +8mA/-70µA at 2.5V +16mA/-90µA at 3.3V
Input Loading: TDO, RTCLK		20pF to ground 10k pull-up to I/O voltage
AC Characteristics		
TCK Frequency		<1 - 40MHz (programmable)
TCK Duty Cycle		40/60% to 60/40%
Target Setup Requirement: TMS, TDI to TCK↑	1.2, 1.4	5ns max at 1.8V
Target Hold Requirement: TMS, TDI after TCK↑	1.2, 1.4	5ns max at 1.8V
Target Output Delay: TCK↓ to TDO	1.3, 1.4	0ns min, 7ns max, at 1.8V

Notes:

1.1: nSRST is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.

1.2: Targets requiring greater setup or hold times on their TMS/TDI inputs may be accommodated by reducing the MAJIC® probe's JTAG interface clock frequency.

1.3: Targets with a slower TDO driver may be accommodated by reducing the MAJIC® probe's JTAG interface clock frequency.

1.4: At higher I/O voltages, the MAJIC® probe's JTAG timing improves and target JTAG requirements are less stringent.

JTAG Interface for MAJIC®/II Series

DC Characteristics	Note	Specification
Target I/O Voltage		1.2v to 3.3v (nominal)
Output Drive: TCK, nTRST, TMS, TDI		± 2mA at 1.2v ± 6mA at 1.8V ± 18mA at 2.5V ± 24mA at 3.3V
Output Drive: nSRST	2.1	+2mA at 1.2v, -120µA at 1.2v +6mA, -180µA at 1.8v +8mA, -250µA at 2.5v +16mA, -330µA at 3.3v
Input Loading: TDO, RTCLK		45pF to ground 10k pull-up to I/O voltage
AC Characteristics		
Max TCK Frequency (75pF load)	2.2	40MHz at 3.3v 20MHz at 1.8v 10MHz at 1.2v
TCK Duty Cycle		40/60% to 60/40%
Target Setup Requirement: TMS, TDI to TCK↑	2.3	4ns max at 3.3v 40MHz
Target Hold Requirement: TMS, TDI after TCK↑	2.3	5ns max at 3.3v 40MHz
Target Output Delay: TCK↓ to TDO	2.4	0ns min, 5ns max, at 3.3v

Notes:

2.1: nSRST is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.

2.2: Maximum frequency is a function of the I/O voltage level vs. capacitive loading. Therefore, the maximum supported frequency may be constrained on low voltage targets, and targets with heavily loaded JTAG pins. The MAJIC® probe's TCK frequency is programmable, from <1 to 40MHz.

2.3: Targets requiring greater setup or hold times on their TMS/TDI inputs may be accommodated by reducing the MAJIC® probe's JTAG interface clock frequency.

2.4: Targets with a slower TDO driver may be accommodated by reducing the JTAG interface clock frequency.

JTAG Interface for MAJIC®/III and MAJICO™

DC Characteristics	Note	Specification
Target I/O Voltage		3.3v (nominal)
Output Drive: TCK, nTRST, TMS, TDI		± 4mA
Output Drive: nSRST	3.1	+1.5mA, -3μA
Input Loading: TDO, RTCLK		30pF to ground 10k pull-up to I/O voltage
AC Characteristics		
TCK Frequency		10MHz
TCK Duty Cycle		40/60% to 60/40%
Target Setup Requirement: TMS, TDI to TCK↑		13ns (max)
Target Hold Requirement: TMS, TDI after TCK↑		26ns (max)
Target Output Delay: TCK↓ to TDO		0ns (min) 86ns (max)

Note:

3.1: nSRST is a pseudo-open-collector output, with a 10k pull-up to the I/O voltage level.

MAJIC$^{PLUS®}$/I With CKP-ARM38 Passive Probe

ETM trace interface requirements for a MAJIC$^{PLUS®}$/I probe with the CKP-ARM38 passive probe.

DC Characteristics	Note	Specification
Target I/O Voltage		2.8V (3.0V nominal) to 3.5V CMOS 3.3V or 5V TTL
Input Loading: TRACECLK	4.1	20pF to ground 1k pull-up to I/O voltage
Input Loading: TRACESYNC, TRACEPKT[0..15], PIPESTAT[0..2]		30pF to ground 10k pull-up to I/O voltage
AC Characteristics		
TRACECLK Frequency		DC - 100MHz
High Time: TRACECLK		4ns min
Low Time: TRACECLK		4ns min
MAJIC® Setup Requirement to TRACECLK↑ for TRACESYNC, TRACEPKT[0..15], PIPESTAT[0..3]		2ns min
MAJIC® Hold Requirement from TRACECLK↑ for TRACESYNC, TRACEPKT[0..15], PIPESTAT[0..3]		2ns min

Note:

4.1: Targets must be capable of driving at least ± 4mA for TRACECLK; a stronger driver (such as ± 8mA) is recommended. The target's TRACECLK drive capability is critical when attempting to capture trace data near the maximum frequency rating.

MAJIC[PLUS®]/I With AP-ARM Active Probes

ETM trace interface requirements for MAJIC[PLUS®]/I with AP-ARM38/A or AP-ARM38+20 active probe.

DC Characteristics	Note	Specification
Target I/O Voltage		1.65V (1.8V nominal) to 3.5V CMOS 3.3V or 5V TTL
Input Loading: TRACECLK	5.1	10pF
Input Loading: TRACESYNC, TRACEPKT[0..7], PIPESTAT[0..2]	5.2	10pF
AC Characteristics		
TRACECLK Frequency		DC - 133MHz in single edge mode DC - 75MHz in ½X (DDR) mode
High Time: TRACECLK		2ns min
Low Time: TRACECLK		2ns min
MAJIC® Setup Requirement to TRACECLK for TRACESYNC, TRACEPKT[0..7], PIPESTAT[0..3]	5,2 5.3	2ns min
MAJIC® Hold Requirement from TRACECLK for TRACESYNC, TRACEPKT[0..7], PIPESTAT[0..3]	5,2 5.3	2ns min

Note:

5.1: Targets must be capable of driving at least ± 4mA for TRACECLK; a stronger driver (such as ± 8mA) is recommended. The target's TRACECLK drive capability is critical when attempting to capture trace data near the maximum frequency rating.

5.2: The MAJIC[PLUS®]/I probe with an AP_ARM38 active probe supports a maximum of eight TRACEPKT data bits.

5.3 In ½X (DDR) mode, timing is relative to both edges of TRACECLK, and TRACECLK is half of the CPU pipeline frequency. In 1X (SDR) clock mode, timing is relative to the rising edge of TRACECLK.

MAJIC$^{PLUS®}$/II With AP2-ARM Active Probes

ETM trace interface requirements for MAJIC$^{PLUS®}$/II with an AP2-ARM active probe.

DC Characteristics	Note	Specification
Target I/O Voltage		1.2v to 3.3v CMOS
Input Loading: TRACECLK	6.1	10pF
Input Loading: TRACESYNC, TRACEPKT[0..15], PIPESTAT[0..2]		10pF
AC Characteristics		
TRACECLK Frequency		DC - 166MHz in single edge mode DC - 82MHz in ½X (DDR) mode DC - 100MHz in demultiplexed mode
High Time: TRACECLK		2ns min
Low Time: TRACECLK		2ns min
MAJIC® Setup Requirement to TRACECLK for TRACESYNC, TRACEPKT[0..15], PIPESTAT[0..2]	6.2	1.6ns min
MAJIC® Hold Requirement from TRACECLK for TRACESYNC, TRACEPKT[0..15], PIPESTAT[0..2]	6.2	1.0ns min

Note:

6.1: Targets must be capable of driving at least ± 4mA for TRACECLK; a stronger driver (such as ± 8mA) is recommended. The target's TRACECLK drive capability is critical when attempting to capture trace data near the maximum frequency rating.

6.2: In ½X (DDR) mode, timing is relative to both edges of TRACECLK, and TRACECLK is half of the CPU pipeline frequency. In 1X (SDR) clock mode, timing is relative to the rising edge of TRACECLK.